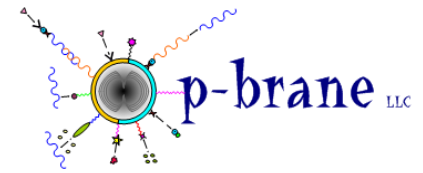


Layout Editor Graphene FET Layout Tutorial

May 28, 2014

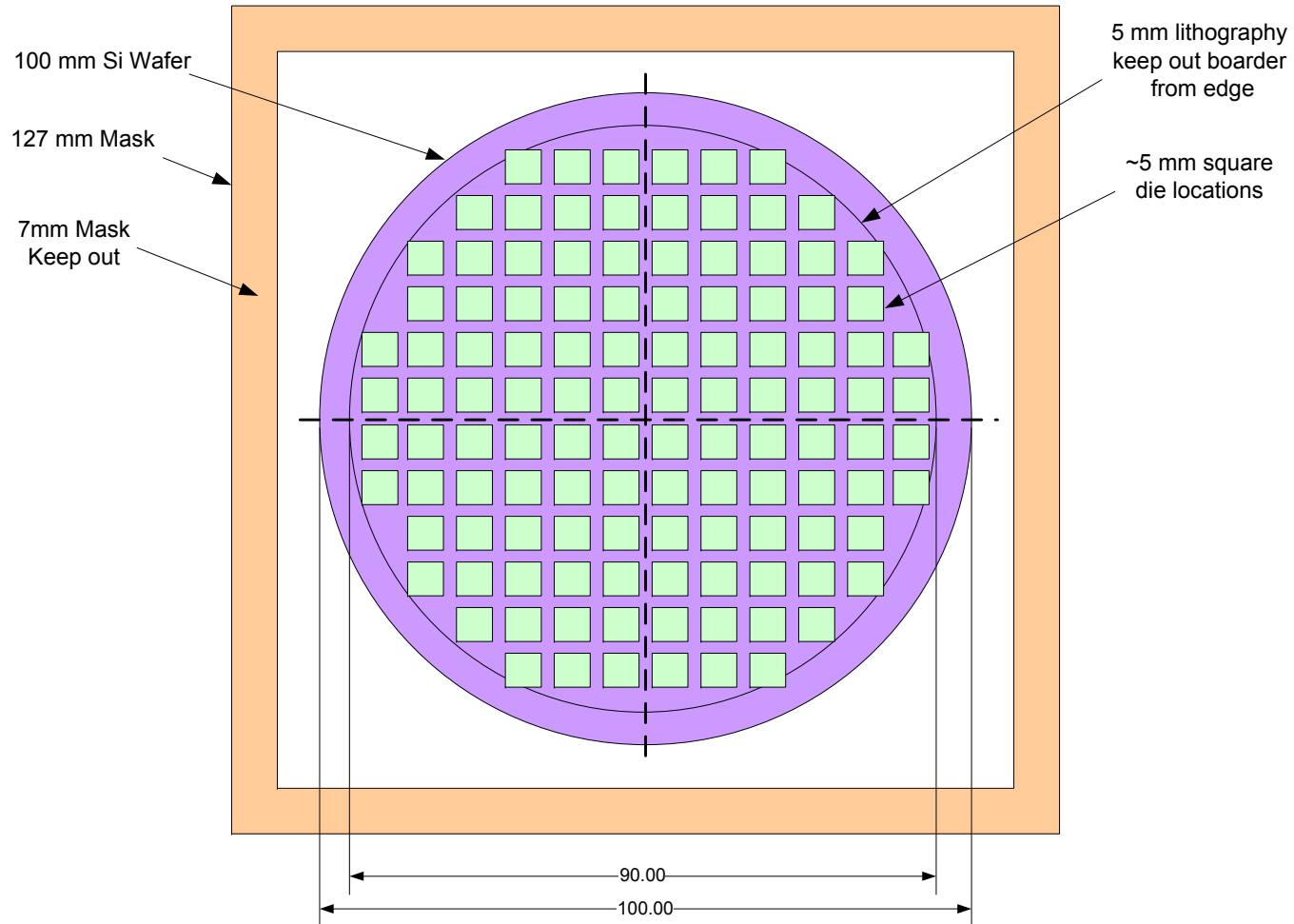
Jay Morreale

Introduction

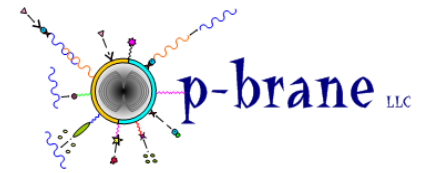


- Graphene FET layout on a 100 mm wafer.

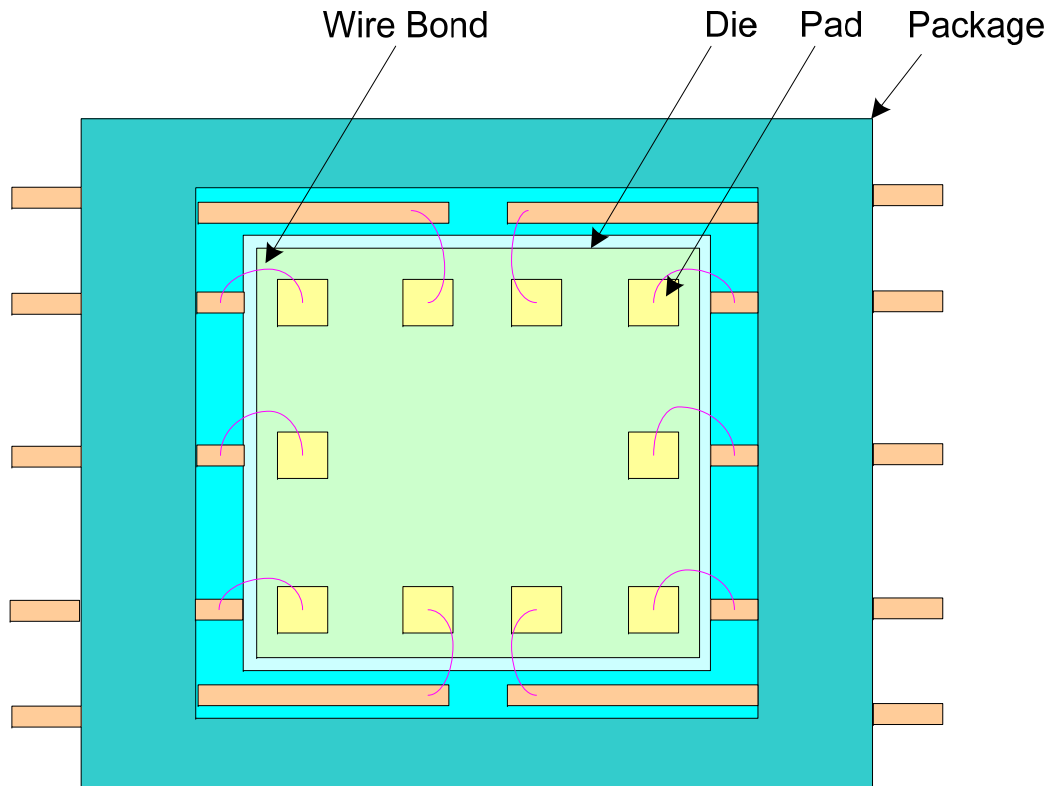
GFET Array Wafer



Die in Package



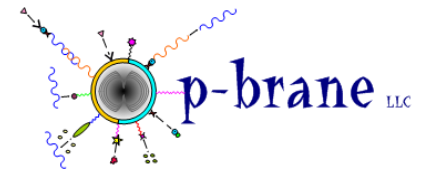
- The die is packaged and the desired GFETs are wire bonded to the pads.



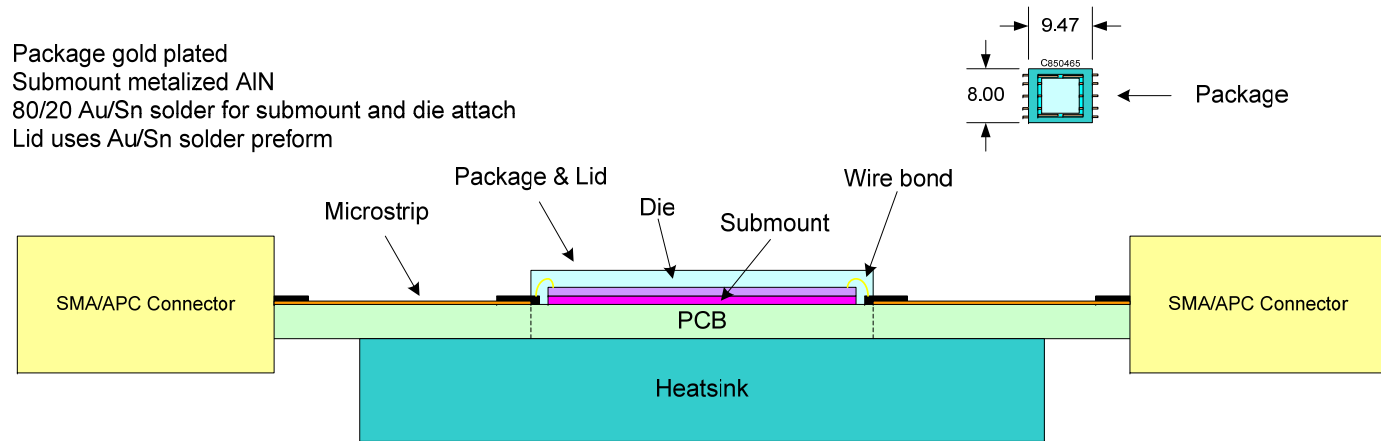
gfet_packaged_c850465.vsd

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Package on PCB



- The GFETs are to be laid out so they can be diced and packaged.
- The packaged GFET is to be placed on a PCB with microstrip traces to RF connectors.

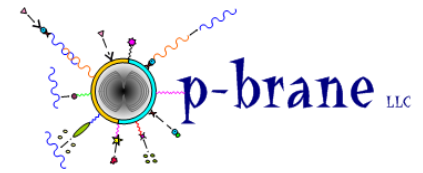


Package gold plated
Submount metalized AlN
80/20 Au/Sn solder for submount and die attach
Lid uses Au/Sn solder preform

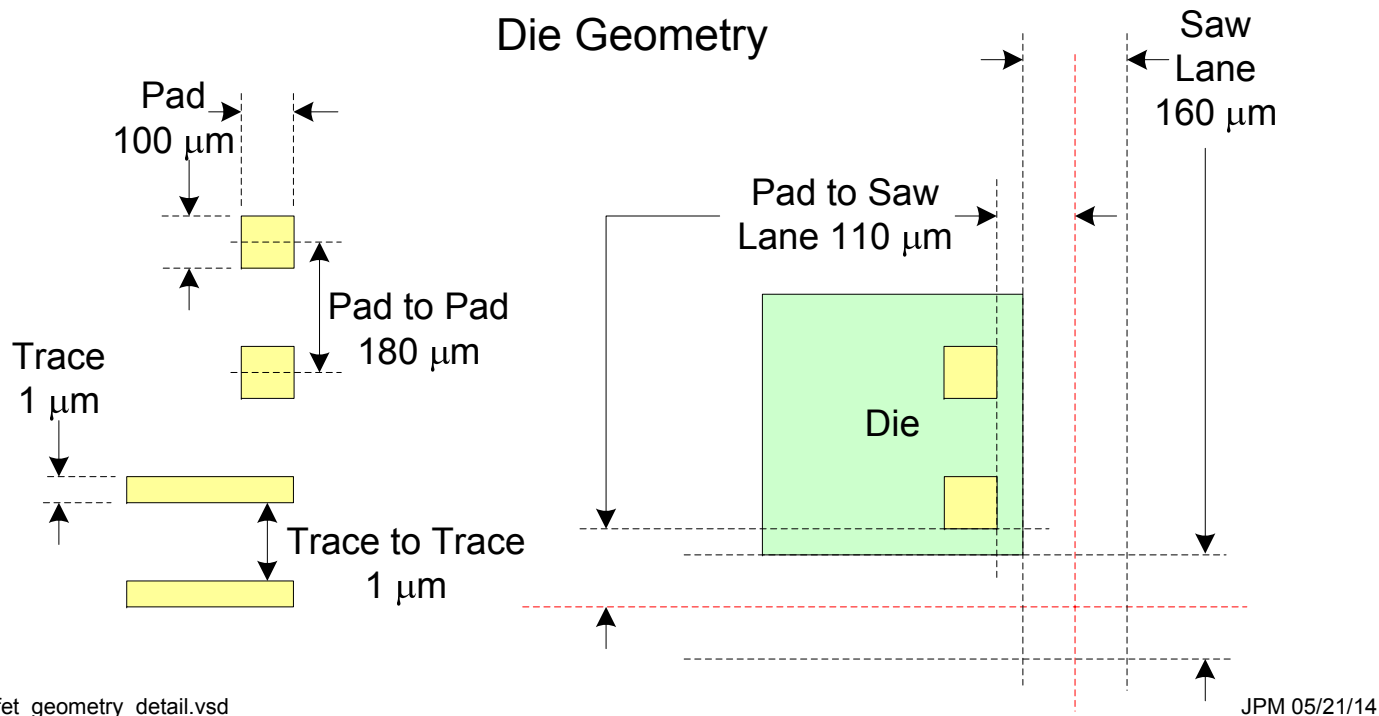
gfet_pgacked_c850465.vsd

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Die Geometry



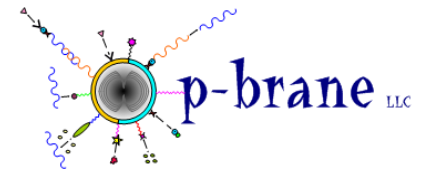
- The tool set defines the minimum die geometry.
- Wire bonder defines minimum pad size.
- Dicing saw defines die spacing.
- Mask resolution sets minimum trace width and spacing.



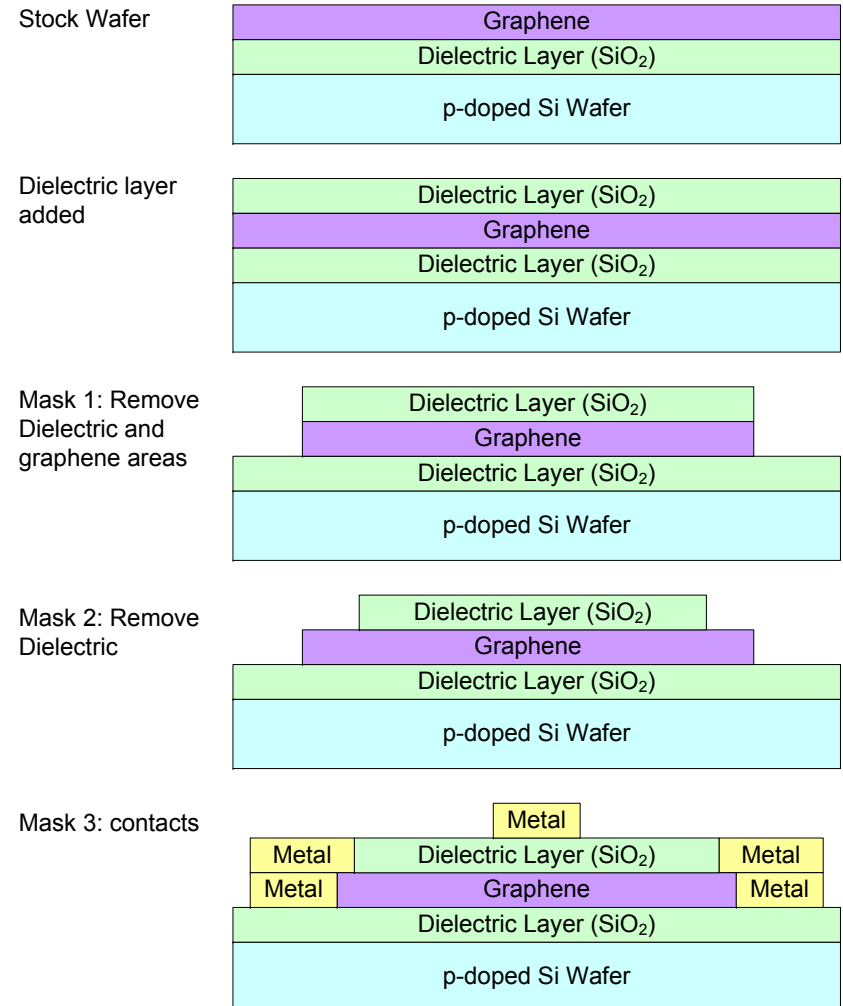
gfet_geometry_detail.vsd

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GFET Stack & Process



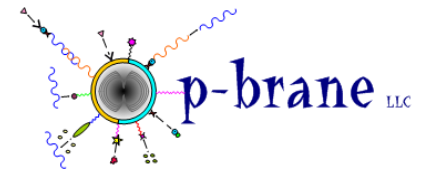
- The process starts with a purchased wafer.
- A dielectric is added on top of the graphene.
- Dielectric and graphene are removed leaving the core device structures.
- Dielectric is removed exposing the graphene.
- Metal contacts are deposited.
- Requires 3 masks.



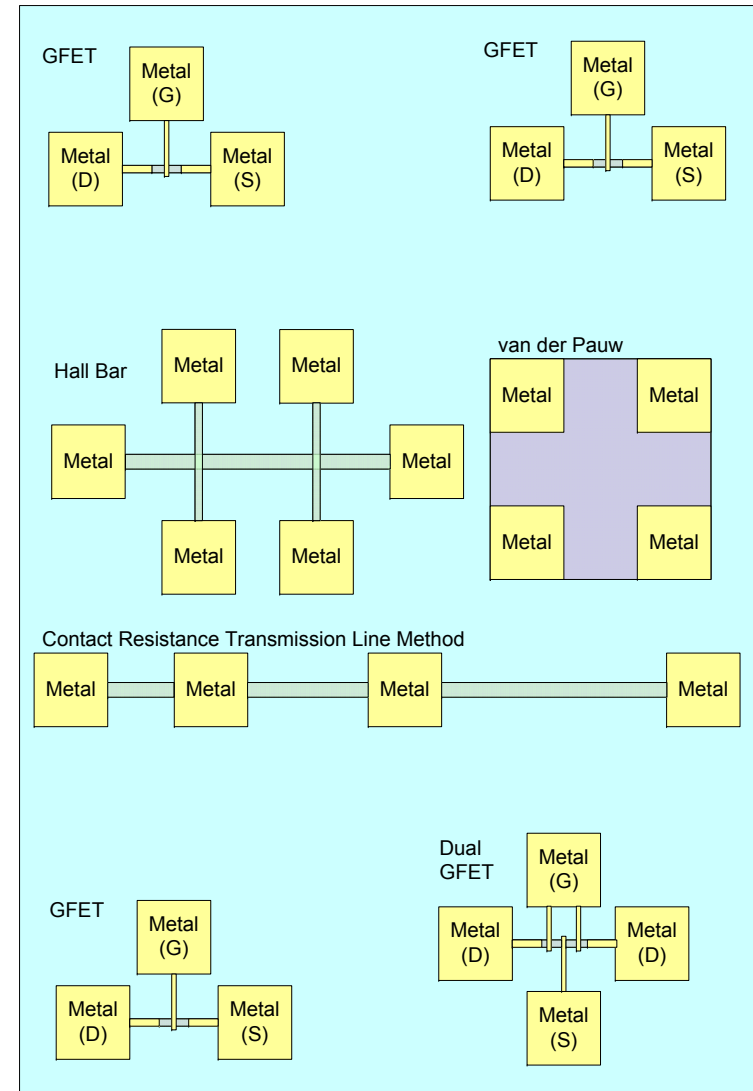
gfet_stack.vsd

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GFET Structures



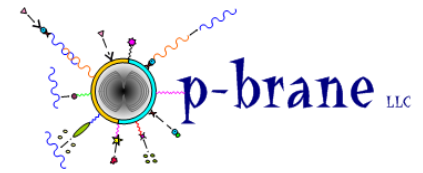
- Multiple devices fabricated
- GFETs
 - GFET
 - Dual GFETs with a common Source
- Test Structure
 - Hall bar
 - van der Pauw
 - Contact resistance structure
 - Helps characterize contacts and graphene to understand GFET performance



gfet_devices.vsd

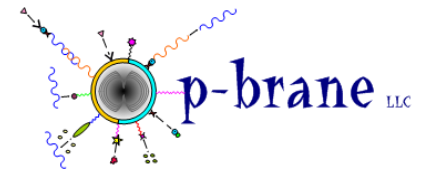
JPM 05/22/14

Tools



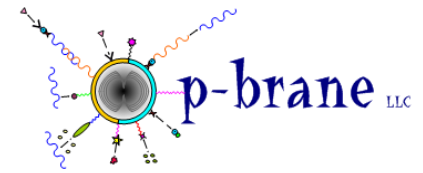
- Suss Microtec contact aligner MA6
- Kulicke and Soffa Model 4526 wire bonder
- Saw-Disco Model 341 dicing saw
- Oxford FlexALRPT Atomic Layer Deposition system (dielectric deposition)
- Denton Infinity 22 E-beam Evaporator (contact deposition)
- Dielectric wet etch
- PVA Tepla 300 Microwave Plasma System (remove graphene)
- Brewer Science CEE Model 100CB Spinner/Hotplate (resist application)

Photoresist



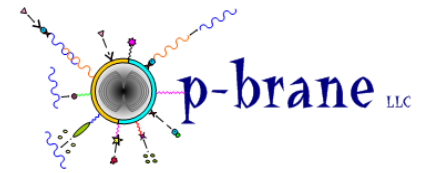
- S1813 positive photoresist
- ~1 μm thick
- Photoresist exposed to UV light through mask gets remove when developed.
- Opening in resist allow removal (etch) or addition (metal deposition) of material.

Materials



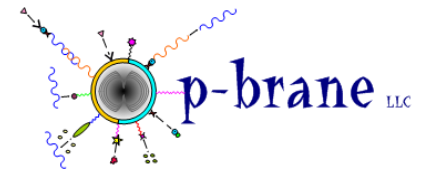
- 100 mm Si/SiO₂ wafer + CVD transferred graphene
 - [2-DTech](#)
 - [Graphenea](#)
 - [Graphene Frontiers](#)
 - [Graphene Supermarket](#) (item appears intermittently)
 - [University Wafers](#)

Masks



- 127 mm (5 inch) Fused Quartz
 - 90 mil
 - Chrome on back
 - 100 nm fracture grid
- Mask 1: Remove dielectric and graphene
- Mask 2: Remove dielectric
- Mask 3: Contacts

References



- [Near-equilibrium Measurements I & 2](#), Mark Lundstrom (2011), ECE 656: Electronic Transport in Semiconductors (Fall 2011)
- [Measuring Metal-Semiconductor Junction Contact Resistance Using the Transmission Line Method \(TLM\)](#)
- [General Rules for Bonding and Packaging](#)